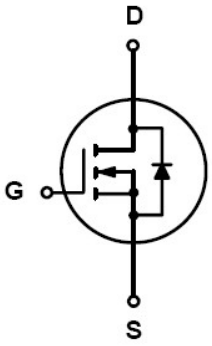
NTR5198N

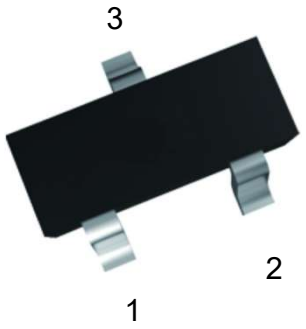
N-Channel Enhancement Power Mosfet Specification

SOT-23

Features
- Advanced trench cell design
- High speed switch

Applications
- Portable appliances
- Notebook/PC appliances
- Power Management
- DC/DC Converter





1：Gate 2：Source 3：Drain

Quick reference
BV ≧ 60 V ID=2.2A
RDS(ON) ≦ 105 mΩ @ VGS = 10 V
RDS(ON) ≦ 130 mΩ @ VGS = 5 V

● Limiting Values

Symbol	Parameter	Rating	Unit
V_{DSS}	Drain-Source Voltage	60	V
V_{GSS}	Gate-Source Voltage	± 20	

- **Electrical Characteristics** (Ta = 25°C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 250 μA	60	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	1.0	1.6	2.5	V
I_{DSS}	Drain Leakage Current	V_{DS} = 48 V, V_{GS} = 0V	-	-	1	μA
		T_J = 85 °C	-	-	30	μA
I_{GSS}	Gate Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	± 100	nA
$R_{DS(ON)}$[a]	On-State Resistance	V_{GS} = 10 V, I_{DS} = 0.5A	-	-	105	mΩ
		V_{GS} = 5 V, I_{DS} = 0.5 A	-	-	130	
Diode Characteristics[b]						
V_{SD}	Diode Forward Voltage	I_{SD} = 0.5 A, V_{GS} = 0V	-	0.7	1.3	V

Notes :

This wafer must be stored at N2 box (RH<20 %).

Wafer must be completely assembled within two months.

a : CP measured on wafer by probe card. ($R_{DS(ON)}$ depended on packaged type and amount of bonding wires)

b : Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2%