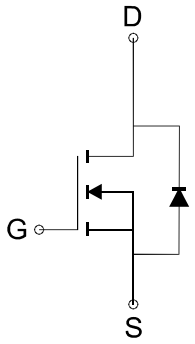
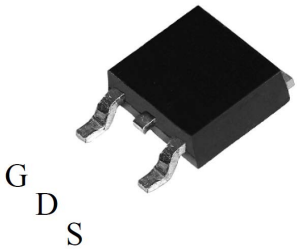
NTD5802NS

N-Channel 40V(D-S) MOSFET

GENERAL DESCRIPTION

The NTD5802NS s the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.





TO-252 N-Channel MOSFET

FEATURES

- $R_{DS(ON)} \leqq 4.4m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 5.7m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- NB/MB Vcore Low side switching
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±10	V
Continuous Drain Current	I_D	34	A

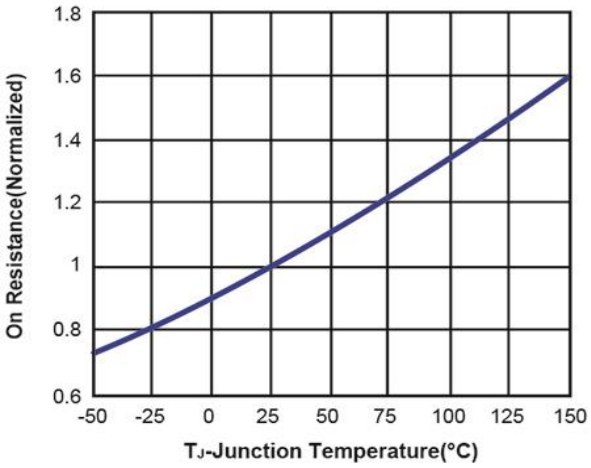
Electrical Characteristics (T_j =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=34A		3.6	4.4	mΩ
		V_{GS}=4.5V, I_D=34A		4.4	5.7	
V_{SD}	Diode Forward Voltage	I_S=25A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=20A		88.9		nC
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=20A		41.4		
Qgs	Gate-Source Charge			14.8		
Qgd	Gate-Drain Charge			16.2		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V,F=1MHz		1442		ns
Coss	Output Capacitance			315		
Crss	Reverse Transfer Capacitance			251		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=15V, R_L =15Ω V_{GS}=10V,R_G=6Ω I_D=1A,		27.3		pF
t_r	Turn-On Rise Time			20.2		
$t_{d(off)}$	Turn-Off Delay Time			108		
t_f	Turn-Off Fall Time			18.4		

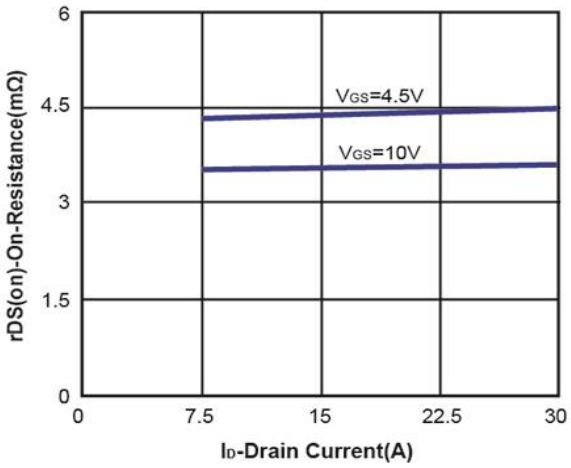
Notes: a. Pulse test; pulse width ≦ 300us, duty cycle ≦ 2%.

Typical Characteristics (T_J =25℃ Noted)

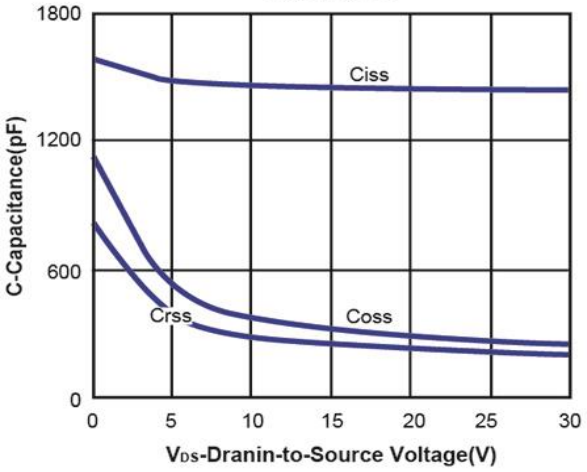
On Resistance vs. Junction Temperature



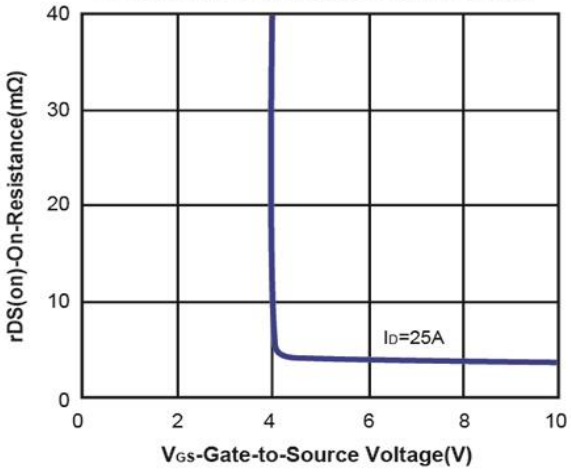
On Resistance vs. Drain Current



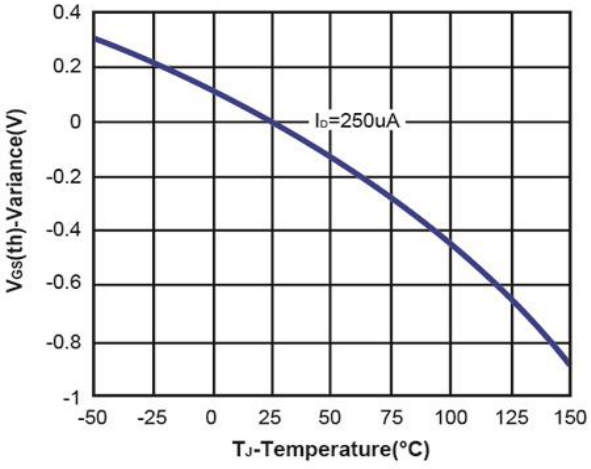
Capacitance



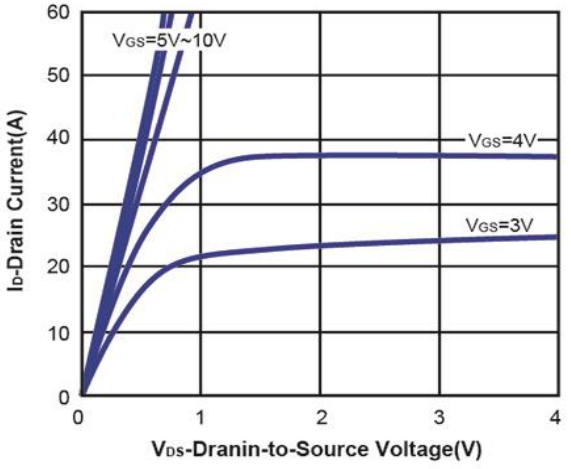
On Resistance vs. Gate-to-Source Voltage



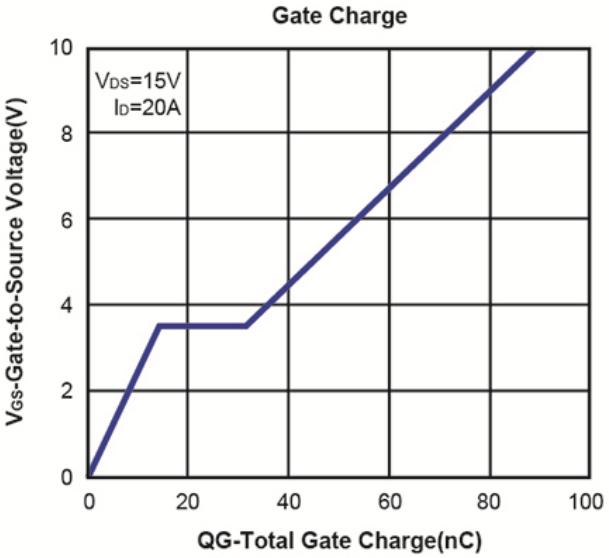
Threshold Voltage

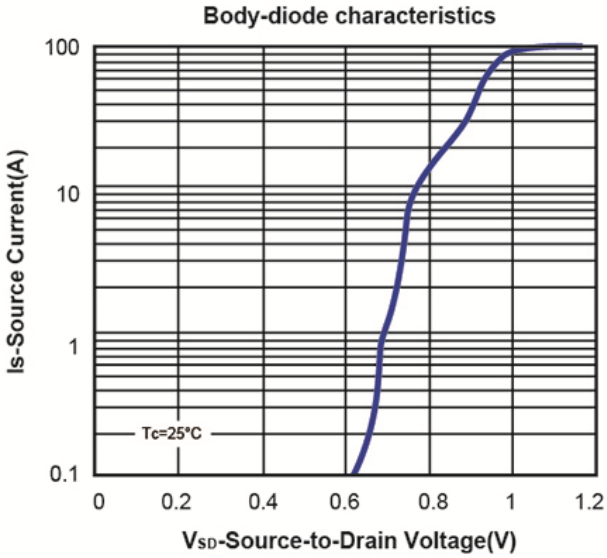


On-Region Characteristics



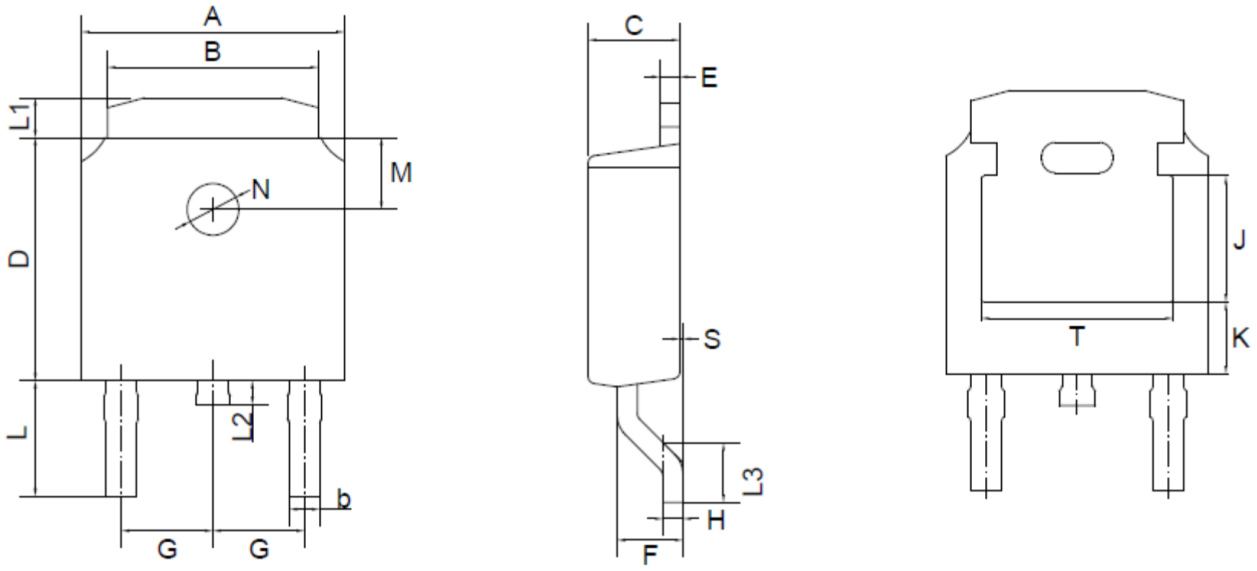
Typical Characteristics (T_J =25℃ Noted)





PACKAGE OUTLINE

TO-252(D-PAK)



TO-252(D-PAK) mechanical data

UNIT		A	B	b	C	D	E	F	G	H	L	L1	L2	L3	S	M	N	J	K	T
mm	max	6.7	5.5	0.8	2.5	6.3	0.6	1.8	2.29 TYPICAL	0.55	3.1	1.2	1.0	1.75	0.1	1.8 TYPICAL	1.3 TYPICAL	3.16 ref.	1.80 ref.	4.83 ref.
	min	6.3	5.1	0.3	2.1	5.9	0.4	1.3		0.45	2.7	0.8	0.6	1.40	0.0					
mil	max	264	217	31	98	248	24	71	90 TYPICAL	22	122	47	39	69	4	71 TYPICAL	51 TYPICAL	124 ref.	71 ref.	190 ref.
	min	248	201	12	83	232	16	51		18	106	31	24	55	0					